CLAIMS:

1. A semiconductor device with a semiconductor body (10) comprising a substrate (11) and a first semiconductor region (1) which lies in the semiconductor body (10), which is of a first conductivity type, which forms a collector region of a bipolar transistor, which is provided with a first connection conductor (6), and above which a second semiconductor region (2) of a second conductivity type opposed to the first is present, forming a base region of the transistor, adjoining the surface of the semiconductor body (10), and being provided at said surface with a second connection conductor (7), and a third semiconductor region (3) which lies recessed in the second semiconductor region (2), which is of the first conductivity type, which forms an emitter region of the transistor, and which is provided with a third connection conductor (8), said device being provided with means for limiting the degree of saturation of the transistor during normal use, characterized in that the second connection conductor (7) is exclusively connected to the second semiconductor region (2) for the purpose of preventing saturation of the transistor, and in that a partial region (2B) of that portion (2A) of the second semiconductor region (2) which lies outside the third semiconductor region (3), as seen in projection, and which lies adjacent the second connection conductor (7) comprises a smaller flux of dopant atoms.

2. A semiconductor device as claimed in claim 1, characterized in that the partial region (2B) of the second semiconductor region (2) has a lower doping concentration.

3. A semiconductor device as claimed in claim 1 or 2, characterized in that the partial region (2B) of the second semiconductor region (2) has a smaller thickness.

4. A semiconductor device as claimed in claim 1, 2 or 3, characterized in that the partial region (2B) of the second semiconductor region (2) is present below the second connection conductor (7).

5. A semiconductor device as claimed in claim 1, 2, 3 or 4, characterized in that a fourth semiconductor region (4) of the first conductivity type is present between the partial region (2B) of the second semiconductor region (2) and the second connection conductor (7), which fourth semiconductor region (4) has a small thickness and a high doping concentration, preferably the same thickness and doping concentration as the third semiconductor region (3).

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6. A method of manufacturing a semiconductor device whereby a first semiconductor region (1) is formed in a semiconductor body (10) comprising a substrate (11), which first semiconductor region (1) lies in the semiconductor body (10), is of a first conductivity type, forms a collector region of a bipolar transistor, and is provided with a first connection conductor (6), whereby a second semiconductor region (2) of a second conductivity type opposed to the first is formed above said first semiconductor region (1), which second semiconductor region (2) forms a base region of the transistor, adjoins the surface of the semiconductor body (10), and is provided with a second connection conductor (7) at said surface, and whereby a third semiconductor region (3) is formed which is recessed into the second semiconductor region (2), which is of the first conductivity type, which forms an emitter region of the transistor, and which is provided with a third connection conductor (8), and whereby the device is provided with means for preventing a saturation of the transistor during normal use, characterized in that the second connection conductor (7) is exclusively connected to the second semiconductor region (2) for preventing a saturation of the transistor, and in that a partial region (2B) of that portion (2A) of the second semiconductor region (2) which lies outside the third semiconductor region (3), as seen in projection, and adjacent the second connection conductor (7) is provided with a smaller flux of dopant atoms.

7. A method as claimed in claim 6, characterized in that the partial region (2B) of the second semiconductor region (2) is formed below the second connection conductor (7) and is given a smaller thickness and a lower doping concentration.

8. A method as claimed in claim 6 or 7, characterized in that the partial region (2B) of the second semiconductor region (2) is given a smaller thickness.

9. A method as claimed in claim 6, 7 or 8, characterized in that the partial region (2B) of the second semiconductor region (2) is formed by means of ion implantation.

10. A method as claimed in claim 6, 7, 8 or 9, characterized in that a thin, strongly doped fourth semiconductor region (4) of the first conductivity type is formed between the partial region (2B) of the second semiconductor region (2) and the second connection conductor (7), preferably simultaneously with the third semiconductor region (3).

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